



White Paper

# **Freescale's e200 Core Family Built on Power Architecture™ Technology**

## Overview and Licensing Model

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# Overview

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Freescale’s e200 family of high-efficiency cores, built on Power Architecture™ technology, is intended for cost-sensitive, embedded real-time performance-driven applications where interrupt responsiveness and low power consumption are important considerations. For example, the e200 core family drives Freescale’s leading MPC5500 family of automotive microcontrollers (MCUs).

Freescale is working with intellectual property (IP) vendor IPextreme to openly license the e200 core family to system-on-chip (SoC) and application-specific standard product (ASSP) designers. The licensable IP products include the e200z0, e200z1, e200z3 and e200z6 cores—all based on Power instruction set architecture (ISA) version 2.03. The compact Power ISA requires minimal silicon investment, allowing designers to employ advanced integration techniques to pack an RISC processor core and multiple peripherals onto a highly functional chip with low power consumption and heat generation characteristics.

With e200 core technology now available to the embedded market, designing SoCs and ASSPs built on Power Architecture technology has never been easier. This white paper reviews the e200 core family technical capabilities and licensing model.

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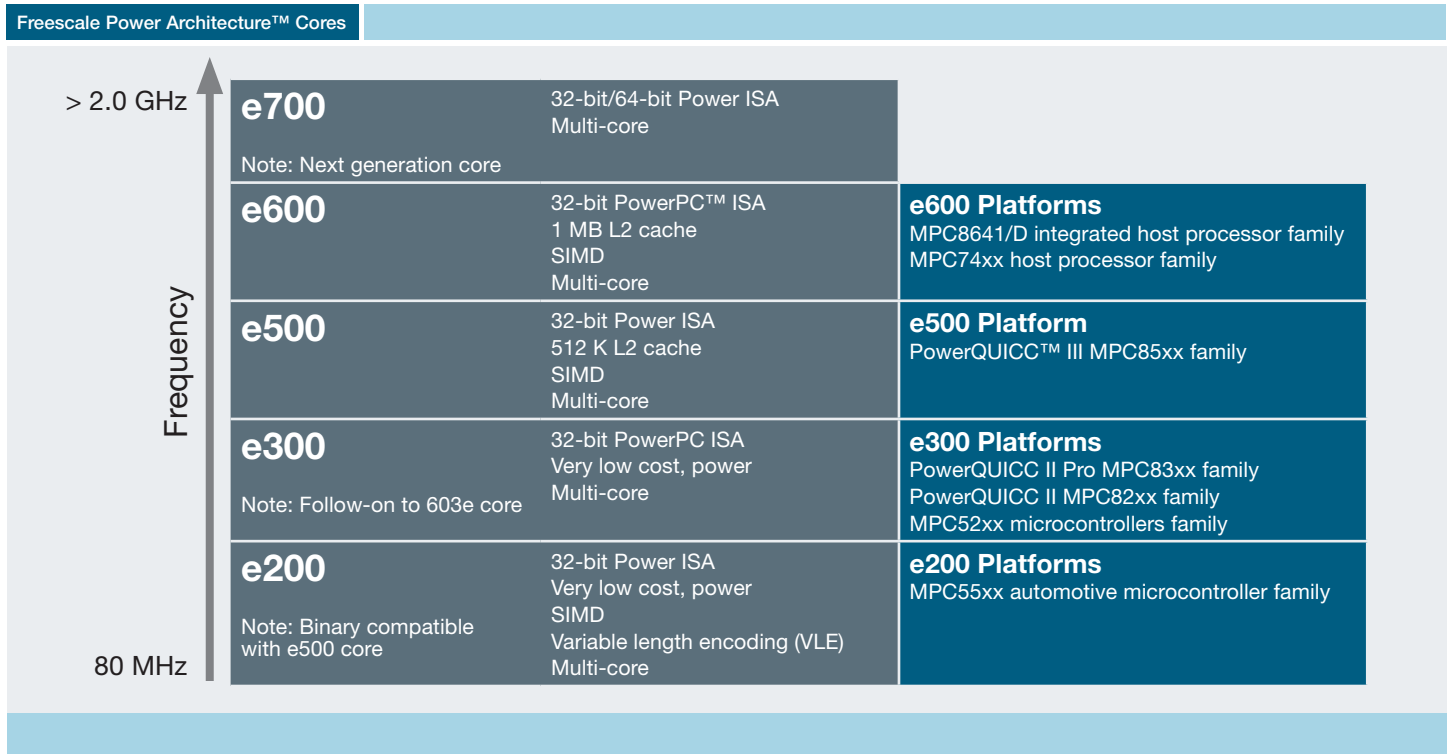
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# 1 Where the e200 Core Family Fits

Power Architecture technology is a scalable, easy to customize and efficient processing architecture. Freescale has a long history of delivering Power Architecture SoC processors and controllers to the market based on its e200, e300, e500 and e600 core families. The breadth of performance embodied in these Freescale cores provides customers with a variety of compatible options to fit their particular application processing needs.



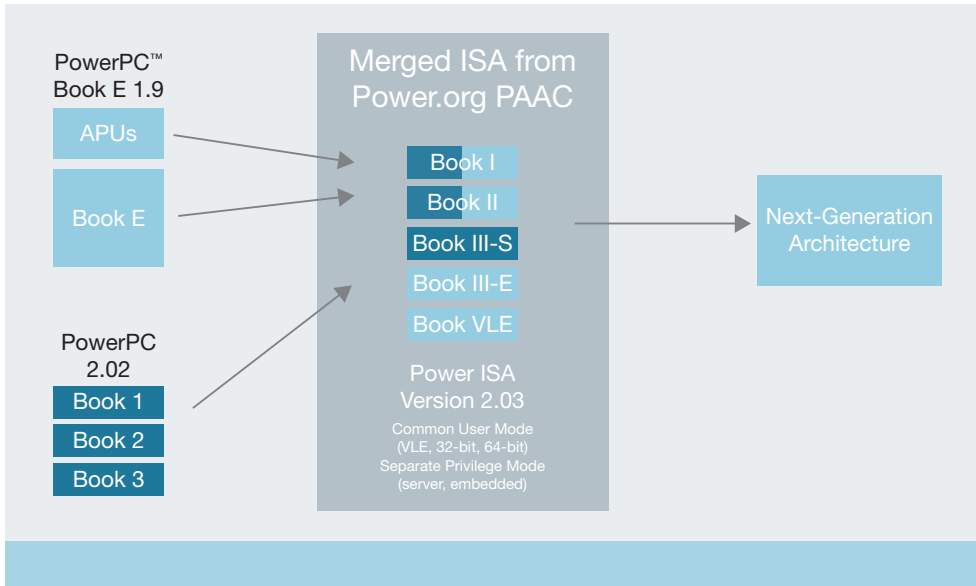
The e200 core family is at the lower end of the performance range of Freescale's extensive Power Architecture core continuum; however, for its target applications, it provides more than enough processing power. The e200 cores currently are leveraged in a wide range of automotive applications, including power management, powertrain control, navigation control, advanced safety systems, and body and chassis control. The e200 cores are also ideal for avionics, robotics, industrial control, medical devices, compact networking solutions, and low-end digital home solutions.

## 2 e200 Core Foundation: Power ISA 2.03

Power Architecture technology is a leading high-performance embedded processor platform with strong industry awareness and support and an extensive existing code base. The ISA generally offers higher performance (per watt and mm<sup>2</sup>) with smaller code footprints than most RISC architectures. The e200z1, e200z3 and e200z6 cores are fully synthesizable, 32-bit integer, user-mode binary compatible devices, implementing Power ISA 2.03, and the e200z0 core implements Variable Length Encoding (VLE) of the Power ISA only.

This Power ISA version is known as the merged architecture because it encompasses the capabilities of existing Power Architecture versions combined into one documentation set. Power ISA 2.03 was designed through proposals from the Power Architecture Advisory Council (PAAC), the organization within the Power.org community dedicated to the management and evolution of the ISA.

## Power ISA Makeup



*Power ISA 2.03 merges previous ISA definitions into one documentation set and serves as the foundation for future generations of the architecture.*

Power ISA is a RISC load/store architecture with separate register sets for integer, floating point and vector operations to enhance processor performance. These register sets include:

- 32 general purpose registers (GPRs) for 32-bit or 64-bit integer operations
- 32 floating point registers (FPRs) for 64-bit floating point operations
- 32 vector registers (VRs) for 128-bit vector operations
- Eight condition register fields (CRs) for 4-bit comparison and flow control

Power ISA also features special registers, including:

- Accumulator (ACC) for accumulation operations
- Counter register (CTR) for efficient loop control
- Link register (LR) for efficient subroutine linkage
- Time base (TBU, TBL) and alternate time base (ATBU, ATBL)
- Status registers (XER, FPSCR, VSCR, SPEFSCR) for providing control and status for various computational operations

Key architectural elements include uniform-length instructions—with the exception of the VLE category, which is a more dense encoding of the base instruction set—a precise exception model and single and double precision floating point IEEE®-754 with additional multiply/add instructions. Vector single instruction multiple data (SIMD) operations on integer and floating point data types provide operations on up to 16 elements in a single instruction.

Power ISA supports separate instruction, data and unified caches with cache operations for block zeroing as well as cache streaming hints. Memory operations are strictly load/store. The flexible memory model allows weakly ordered memory accesses for enhanced performance and supports both big- and little-endian addressing, with separate categories for molded (server) and per-page (embedded) endianness.

## 2.1 Power ISA 2.03 VLE Extension

The VLE category exemplifies the breadth and adaptability of the Power Architecture model. VLE redefines encodings for many user instruction set architecture (UIA)-based instructions to fit into 16-bit opcodes. This approach allows the UIA to be introduced into environments that require a small code footprint and offers more efficient binary representations for embedded processors. This alternate encoding can not only reduce overall system cost but also can improve code performance by up to 30 percent over the standard Power ISA.

Rather than defining an entirely different ISA or supplanting the Power ISA, the VLE extension serves as a supplement that can improve code density to an application or to part of an application. The e200z0 core only implements the VLE instructions while the other cores may implement both the standard 32-bit Power ISA instructions as well as VLE.

The VLE set of alternate encodings is selected on an instruction-page basis. A single page-attribute bit selects between standard instruction encodings and VLE instructions for that page of memory. Pages of either configuration can be intermixed freely, allowing a combination of both types of encodings in an application. Instruction encodings in instruction pages marked as using the VLE extension are either 16- or 32-bits long and are aligned on 16-bit boundaries. Therefore, all pages marked as VLE must use big-endian byte ordering.

The programming model uses the same register set with both instruction encodings, although certain registers are not accessible by VLE instructions using the 16-bit formats. Not all CRs are used by condition setting or conditional branch instructions executing from a VLE instruction page. Furthermore, immediate fields and displacements differ in size and use due to more restrictive encodings imposed by VLE instructions.

Other than requiring big-endian byte ordering for instruction pages and the additional page attribute to identify whether the instruction page corresponds to a VLE section of code, VLE complies with the embedded category memory model. Likewise, the VLE extension complies with the Book III-E definitions of the exception and interrupt models, timer facilities, debug facilities and special-purpose registers (SPRs).

## 2.2 Power ISA 2.03 Signal Processing Engine (SPE)

The SPE supports real-time fixed-point and single-precision embedded numerics operations using the general-purpose registers. All arithmetic instructions that execute in the core operate on data in the GPRs, which have been extended to 64-bits to support SIMD vector instructions defined by the SPE category. These instructions operate on a vector pair of 16-bit or 32-bit data types and deliver vector and scalar results.

# 3 e200 Core Family Characteristics

Freescale's e200 family of synthesizable, high-efficiency cores, built on Power Architecture technology, is designed for cost-sensitive, embedded real-time applications. The licensable e200 cores include four versions of the e200 core family: the e200z0, e200z1, e200z3 and e200z6 cores. In 90 nm CMOS process technology, these cores range from 150 MHz to 300 MHz in performance. The cores offer low interrupt latency, low-power design through clock gating, variable cache sizes, variable MMU sizes, standard Nexus debug interface and an AMBA® AHB™ bus interface unit. The cores also may include Power ISA 2.03 features, such as SPE, single-precision floating-point unit (FPU) and VLE technology.

e200 Cores Available for Licensing			
e200z0	e200z1	e200z3	e200z6
150 MHz	150 MHz	150 MHz	300 MHz
4-stage	4-stage	4-stage	7-stage
VLE	VLE/32-bit	VLE/32-bit	VLE/32-bit
	MMU	MMU	MMU
		FPU	FPU
		SPE	SPE
			Up to 32K L1

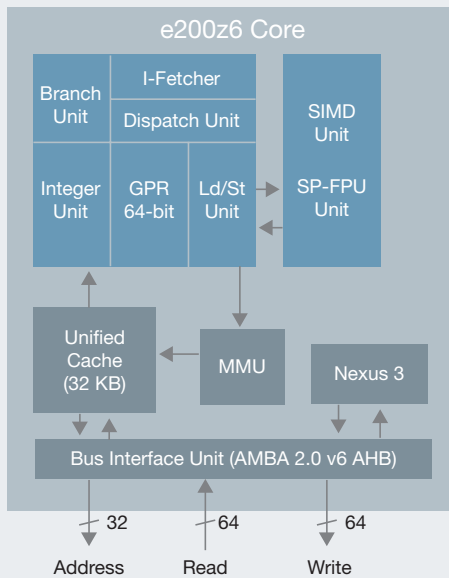
Note: Core frequency based on 90 nm process technology estimates

*The Freescale e200 core family effectively addresses the needs of automotive, consumer, networking and industrial applications with increased system performance requirements in complex, real-time environments.*

The e200z0, z1 and z3 cores each have a compact four-stage pipeline. The small-footprint z0, in particular, is designed to run the VLE instruction set only, which delivers a high level of code density, reducing memory requirements. The z1 and z3 cores feature a memory management unit (MMU) and the full 32-bit instruction set. For applications with significant signal processing requirements, the z3 core includes SPE and FPU functionality, which minimize the need for an additional DSP. It can also function effectively without any cache, sharply reducing silicon area for cost-sensitive applications.

The e200z6 core, the highest-performing licensable Power Architecture core of the e200 family, has a single issue, seven-stage pipeline and all of the features of the z3 core, plus a unified 32 Kb, 8-way set-associative cache. The e200z6 core provides SPE, FPU and optional VLE capabilities. Its performance levels can also easily drive a number of advanced IP blocks that may be integrated in an SoC solution.

e200z6 Core Block Diagram



It's important for core IP to easily interact with other sub-systems and peripherals in an SoC design. To that end, the e200 core leverages a standard AMBA bus to interface with other feature blocks. The AMBA protocol is an open standard, on-chip bus specification that details a strategy for the interconnection and management of functional blocks that makes up an SoC. The standard AMBA bus enables developers to leverage the extensive ARM peripheral IP ecosystem and libraries and bring Power Architecture compatibility and performance to existing SoC architectures. Another important note for embedded developers is that the e200 core family implements a standard Nexus debug interface (IEEE-ISTO 5001™)—static debug through Nexus1 and real time debug through Nexus2/3. Although the tough requirements of automotive powertrain applications were the impetus for the standard, it has become a general purpose debug interface for a variety of embedded applications.

Each e200 core is supported by an extensive development ecosystem that includes compilers, debuggers, real-time operating systems, reference boards, application code and EDA tools.

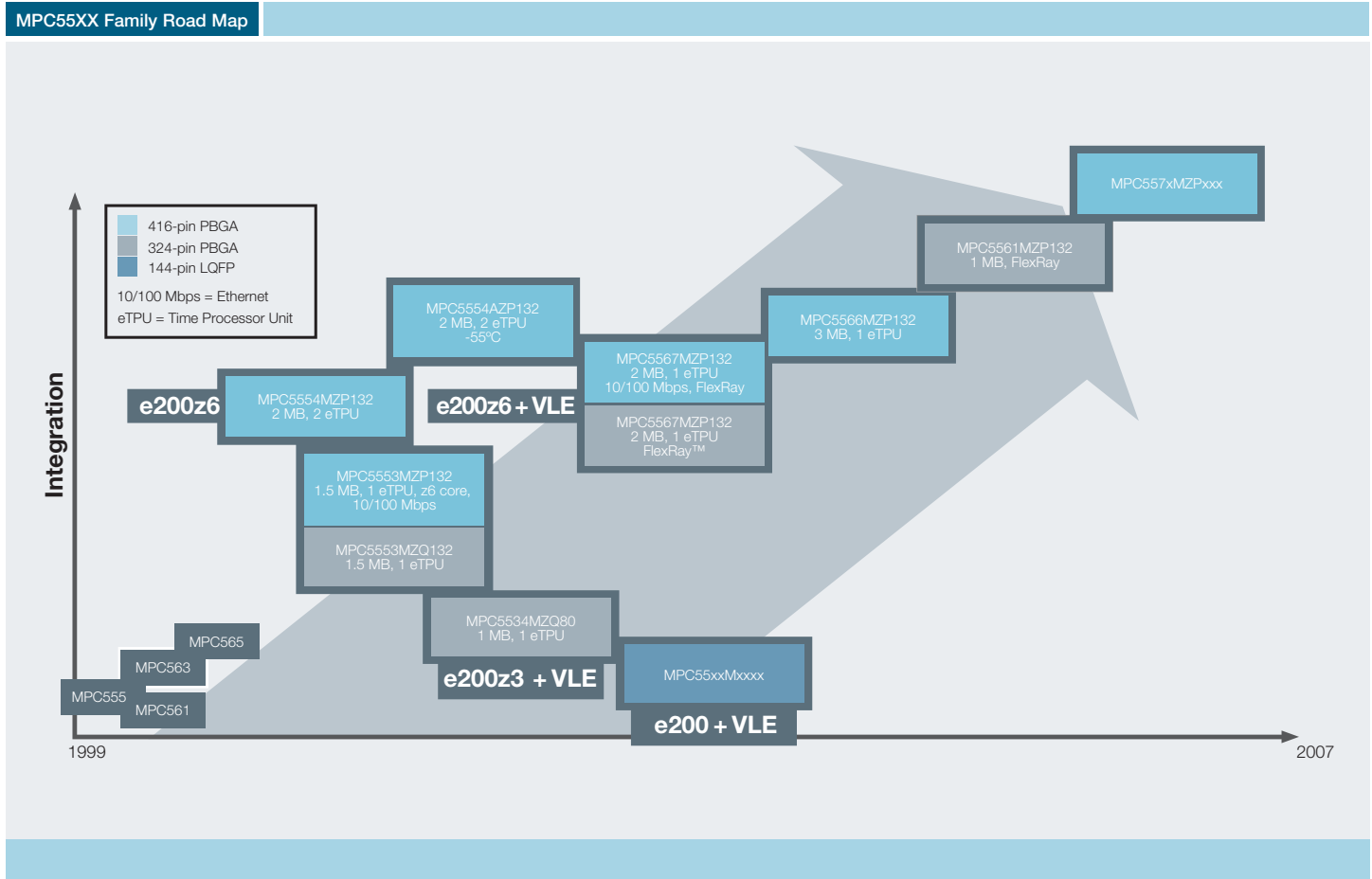


## 4 e200 Core SoC Example: MPC55xx Family

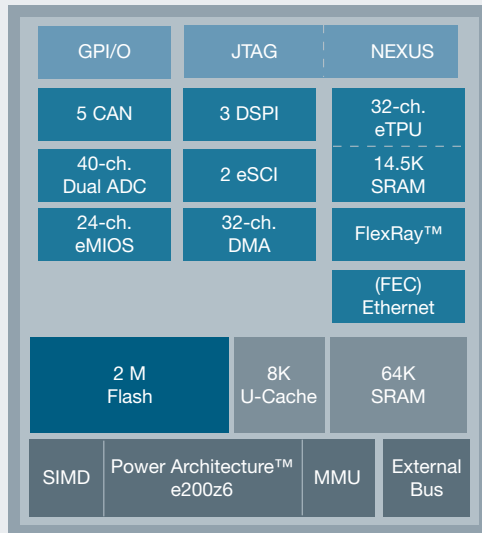
The MPC55xx family of 32-bit automotive microcontrollers is powered by e200 cores built on Power Architecture technology and provides high-performance processing and connectivity solutions for a wide range of automotive and industrial control applications. Offering pin compatibility throughout the entire flashed-based family, engineers are given the ability to migrate their efforts from one design to another, reducing development costs and improving time to market. MPC55xx family members include:

- MPC5567 (e200z6 core) with extensive connectivity options for next-generation automotive applications, such as advanced chassis
- MPC5566 (e200z6 core) for powertrain control, offering up to 3 MB flash memory
- MPC5561 (e200z6 core) for advanced safety applications
- MPC5510 (e200z1 core plus optional e200z0 core) for cost-sensitive body applications

To date, Freescale has shipped more than one million e200 core-based MPC55xx family microcontrollers with zero-defect quality.



The MPC5567 combines the high performance characteristics of the e200z6 core architecture with high-level module functions, including FlexRay™ technology, 10/100 Ethernet and enhanced Time Processor Unit (eTPU). The MPC5567 is particularly well suited for next-generation automotive applications because the FlexRay network will play a significant role in advanced chassis applications, such as stability control and brake-by-wire and steer-by-wire systems.



With the combined capabilities of FlexRay technology and Ethernet, along with five Controller Area Network (CAN) modules, the MPC5567 helps developers control costs when designing increasingly complex applications in automotive and industrial systems, such as:

- Multi-point fuel injection
- Electronically controlled transmissions
- Direct diesel injection
- Gasoline direct injection
- Autonomous vehicles
- Avionics
- Robotics
- Motion control
- Turbine control
- Utilities/power management
- Alternative energy management

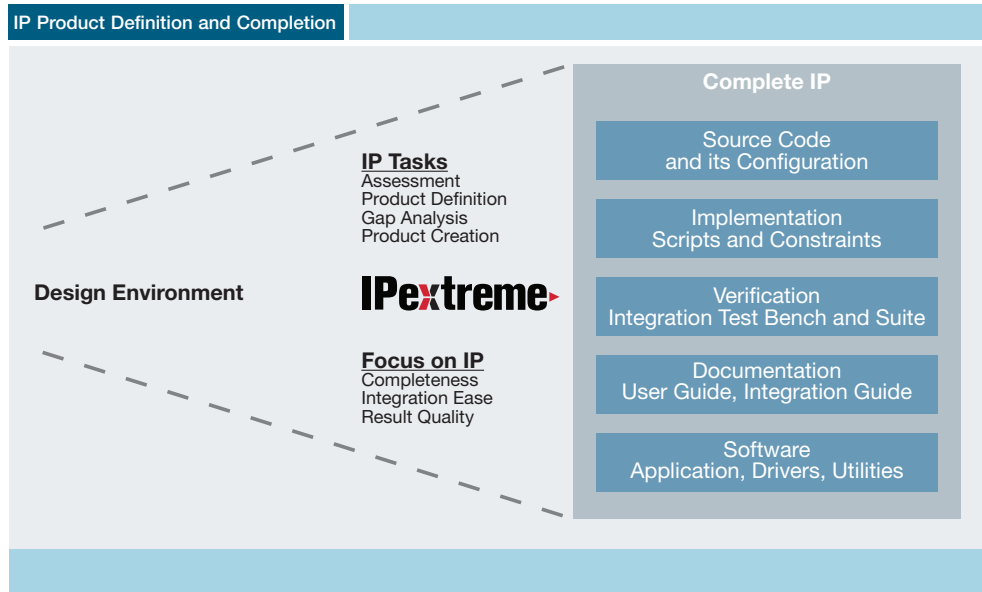
Another member of the MPC5500 family, the MPC5510 microcontroller, uses the capabilities of two e200 cores, the e200z1 core with an optional e200z0 core. The MPC5510 family is designed to reduce the number of electronic control modules in the automotive cockpit by integrating body electronics control, such as lights, wipers, seats and windows, with gateway functions between CAN, Local Interconnect Network (LIN) and FlexRay networks.

## 5 e200 Core Licensing Program

Freescale is licensing its e200 core IP, built on Power Architecture technology, through collaboration with IPextreme, bringing Power Architecture performance and compatibility to a wide range of SoC and ASSP designs. IPextreme, a long-time partner to Freescale and fellow member of Power.org, commercializes the e200 core IP, making it straight-forward to integrate into customers' chip designs.

The e200 IP family available through IPextreme currently includes four core variants: e200z0, e200z1, e200z3 and e200z6. Customers licensing the e200 cores through IPextreme will be provided with the complete IP, including the source code, scripts, integration test, documentation and additional software necessary for full implementation. IPextreme's packaging is EDA-neutral, enabling developers to use the tools and process of their choice. IPextreme also provides expert customer support and maintenance for the e200 core technology.

By making Power Architecture core technology available through IPextreme, Freescale is opening up the opportunities for chip designers to leverage this world-class architecture in a wide assortment of embedded solutions that are also compatible with Power Architecture standard products available in the marketplace today.



*IPextreme markets sell and support the synthesizable e200 cores with complete IP to embedded designers who intend to integrate the cores into SoC or ASSP products targeting the automotive, consumer, industrial and networking markets.*

## 6 Conclusion

Power Architecture technology prevails in a wide array of embedded, automotive and enterprise markets and continues to grow in the competitive marketplace because it is a single architecture that scales from very low to very high performance. It supports converging technologies, enables collaboration across industries and opens the doors to new innovations. The Power ISA is managed openly by the Power Architecture Advisory Council (PAAC) within Power.org, building new levels of extensibility and compatibility throughout the microprocessor and microcontroller development community.

Freescale takes full advantage of the scalable Power ISA to create feature-rich e200 core products for a large and growing Power Architecture customer base. Collaborating with IPextreme to license the e200 core IP ensures that more designers have access to the products and knowledge that will further expand the reach of Power Architecture technology.

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